

High-Speed Information Processing

U T A H S T A T E U N I V E R S I T Y

CENTER

This center is driving the creation of smaller, cheaper and faster chips to run miniature digital devices, by commercializing fast algorithm technologies for specific families of high-speed integrated circuit (IC) chips. When implemented in IC chips, fast algorithms add great value to chip designers, manufacturers, and OEMs because their products are cheaper, faster, smaller, and less power hungry than those with standard algorithms that use multipliers and large amounts of memory. Additional benefits flow from faster design cycles, compact implementation and low-cost hardware.

TECHNOLOGY

The center holds rights to several technologies such as: multiplier-free digital filters: design methodology and architecture; multiplier-free algorithms for hyperspectral image restoration and compression; full-duplex echo canceller: algorithm and architecture; feedback cancellation algorithms for hearing aids.; Fast Integer Fourier Transform (FIFT).

ACCOMPLISHMENTS

Patents are pending on the full-duplex echo canceller and on the multiplier-free digital filter design. The Center developed a full-duplex echo canceller that enables natural, lifelike conversations with speaker phones and never cuts off or enters half-duplex mode. They implemented the new echo canceller on a digital signal processing (DSP) chip that can be put into speaker phones for the home or office, and licensed the technology to a new Utah company, SP Communications, that plans to enter both the cell phone and speaker phone markets. A larger existing (confidential) Utah firm is funding work and incorporating related technology into their products as well.

THINK TANK

What if there was...



**A way to have
face-to-face like
conversations with
a speaker phone
without those
annoying echoes
and cut offs???**

**Tamal Bose
Utah State University
Electrical & Computer
Engineering
4120 Old Main Hill
Logan, UT 84322
435-797-7227
tamal.bose@ece.usu.edu**